AAC CLYDE SPACE

Command & Data Handling

SIRIUS OBC LEON3FT

Designed for advanced satellite constellations in LEO and deep space exploration missions the readily available Sirius OBC with LEON3FT delivers 'always on' reliable operations that work every time on time with precision performance. With enhanced error detection and correction, the Sirius OBC is tolerant to Single-Event-Effects (SEE) in logic and data storage. Fault tolerance is secured through TMR (Triple-Modular Redundancy) on all FPGA flip-flops and through boot flash and EDAC (error detection and correction) on memories.

Sirius spacecraft avionics are modular in design, modules can be combined to offer redundant configurations or to simply accommodate mission specific requirements. The Sirius Command and Data Handling system has a standard single string system that consists of an on-board computer (Sirius OBC) and a combined mass memory with CCSDS stack (Sirius TCM). The OBC runs mission specific software and manage the spacecraft system. The TCM receives and stores payload data and platform housekeeping data while at the same time distributing telecommands and serving mass memory data to the transceiver.

PERFORMANCE

With 50 MHz LEON3FT fault-tolerant soft processor, its RTEMS real-time operating system (RTOS) is compliant to IEEE 1754 SPARCv8. Utilizing SpaceWire on-board the main data bus, the on-board computer is designed to emphasis high performance, resilience and reliability.

RELIABILITY

Sirius OBC solutions have autonomous single event latch-up protection in logic and data storage. Our inbuilt protections are based on over a decade of design heritage guarantee realtime-on-time operations. Designed and qualified for five years in LEO.

MODULARITY

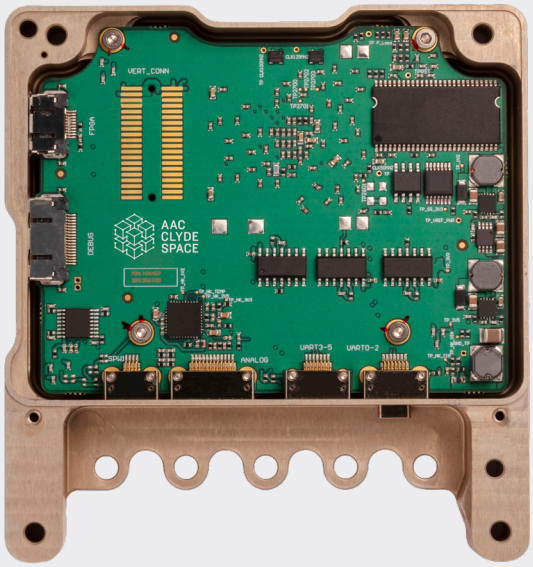
Designed for the most demanding missions the Sirius OBC provides modular, satellite compatible, mechanical design. With pulse commands for low level, basic commanding.

TECHNICAL SPECIFICATIONS

General	
Expected	5 years in LEO
Processor	32-bit LEON3FT (IEEE-1754 SPARC v8) fault-tolerant processor
FPU	IEEE-754 single/double precision FPU
Processor Clock	50 MHz
SCET	15.25 µs accuracy
SDRAM	64 MB (post-EDAC)
Instruction Cache	8 kB
Data Cache	8 kB
NVRAM	16 kB (post-EDAC)
Operating Temperating Range	-30°C to +60°C
Nonvolatile System Memory Nand Flash	2 GB (post-EDAC)
Power Supply Input	4.5 V to 16 V
Radiation (TiD)	20 kRAD (qualified >30 kRAD, Si)

Interfaces		
SpaceWire	50 Mbps	2
Serial Ports	RS422 / RS485 UARTs	6
Serial Ports	RS485-only UARTs	2
PSS Interface	RS485 PPS input / output	1/1
Analog Input Buffered	24 bit, up to 31250 SPS	8
GPIO	3.3 V logic	16
Debugging	JTAG port for CPU debugging via GRMON/GDB	1
CAN	Implemented on optional daughter board	2
SpaceWire	Implemented on daughter board	2

Size, Weight & Power	
Nominal Power Consumption	1.3 W
Mass	130 g
Length	95.89 mm
Width	90.17 mm
Height	17.20 mm
Height - Optional daughter board	12.50 mm



To make an enquiry, request a quotation or learn about AAC Clyde Space's other products and services, please contact:
enquiries@aac-clydespace.com

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